AOZ8300

Ultra-Low Capacitance TVS Diode Array

General Description

The AOZ8300 is a transient voltage suppressor array designed to protect high speed data lines from ESD and lightning.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. They AOZ8300 may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The TVS diodes provide effective suppression of ESD voltages: ±15 kV (air discharge) and ±8 kV (contact discharge).

The AOZ8300 comes in a Halogen Free and RoHS compliant, SOT-23 package and is rated over a -40 °C to +85 °C ambient temperature range. Both packages are compatible with lead free and SnPb assembly techniques. The small size, low capacitance, and high ESD protection makes the AOZ8300 ideal for protecting high speed video and data communication interfaces.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±30 kV (air discharge) and ±30 kV (contact discharge)
  - IEC 61000-4-5 (Lightning) 20 A (8/20 µs)
  - IEC 61000-4-4 (EFT) 40 A (5/50 ns)
  - Human Body Model (HBM) ±24 kV
- Protects four I/O lines
- Low clamping voltage

Applications

- USB 2.0 power and data line protection
- Video graphics cards
- Monitors and flat panel displays
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Green Product

Typical Application

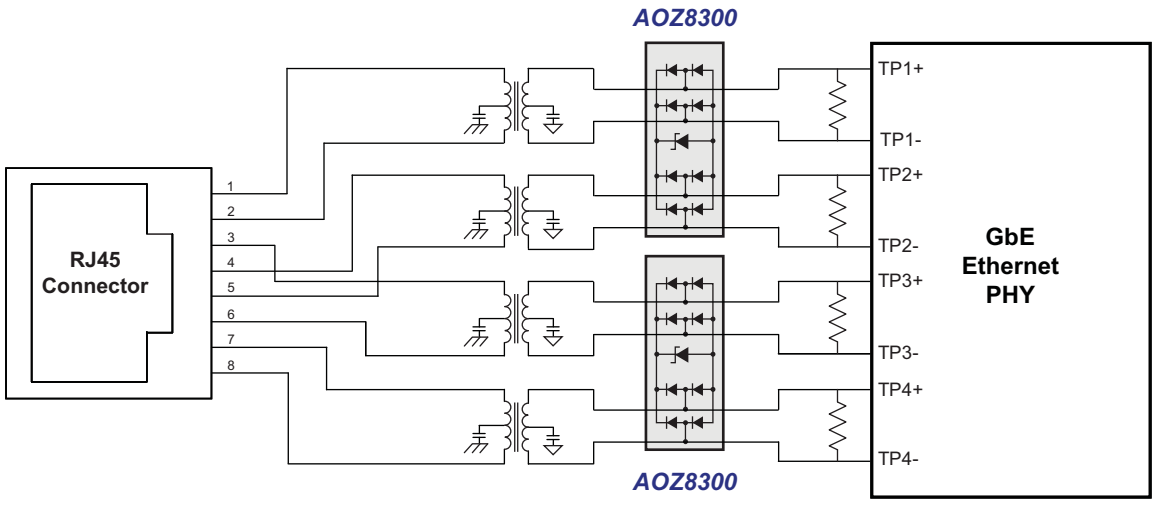


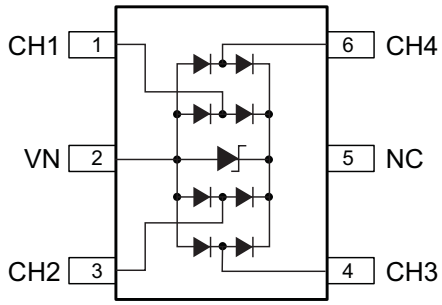
Figure 1. 10/100/1000 Ethernet Port Connection

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8300CI-05	-40 °C to +85 °C	SOT23-6	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



SOT23-6
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Peak Pulse Current (I_{PP}), t_P = 8/20 µs	20 A
Peak Power Dissipation (8 x 20 µs @ 25 °C)	450 W
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating per IEC61000-4-2, Contact[1]	±30 kV
ESD Rating per IEC61000-4-2, Air[1]	±30 kV
ESD Rating per Human Body Model[2]	±30 kV

Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C

Electrical Characteristics

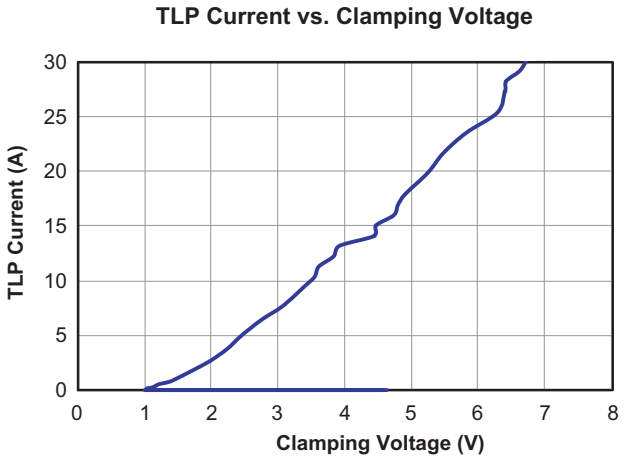
T_A = 25°C unless otherwise specified.

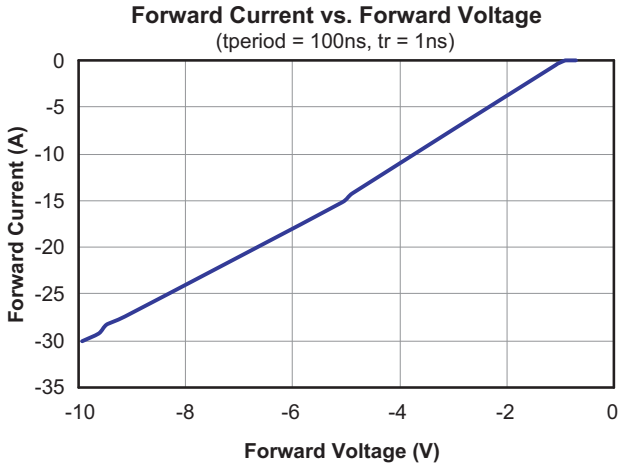
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between I/O and VIN[4]			2.5	V
V_{BR}	Reverse Breakdown Voltage	I_T = 100 µA, between I/O and VIN[5]	2.8			V
I_R	Reverse Leakage Current	V_{RWM} = 2.5 V, between I/O and VIN			0.1	µA
V_F	Diode Forward Voltage	I_F = 15 mA	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5 A, tp = 100 ns, any I/O pin to Ground[3][6]			 3.5 -3.5	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 10 A, tp = 100 ns, any I/O pin to Ground[3][6]			 4.5 -5	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 30 A, tp = 100 ns, any I/O pin to Ground[3][6]			 9 -12	 V V
C_j	Junction Capacitance	V_R = 0 V, f = 1 MHz, any I/O pin to Ground		2.5	3.5	pF
ΔC_j	Channel Input Capacitance Matching	V_R = 0 V, f = 1 MHz, between I/O pins[3]			0.2	pF

Notes:

3. These specifications are guaranteed by design.
4. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
5. V_{BR} is measured at the pulse test current I_T.
6. Measurements performed using a 100 ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics





Application Information

The AOZ8300 TVS is design to protect up to four data lines from damaging transient over-voltage by clamping the voltage to a reference. When the transient on a protected data line exceeds the reference voltage, the steering diode is forward bias thereby conducting the harmful ESD transient away from the sensitive circuitry under protection.

PCB Layout Guidelines

Printed circuit board layout is key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the most important design consideration. The AOZ8300 devices should be located as close as possible to the noise source. AOZ8300 devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8300 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse is coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8300 device. Long signal traces will act as antennas and receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced.

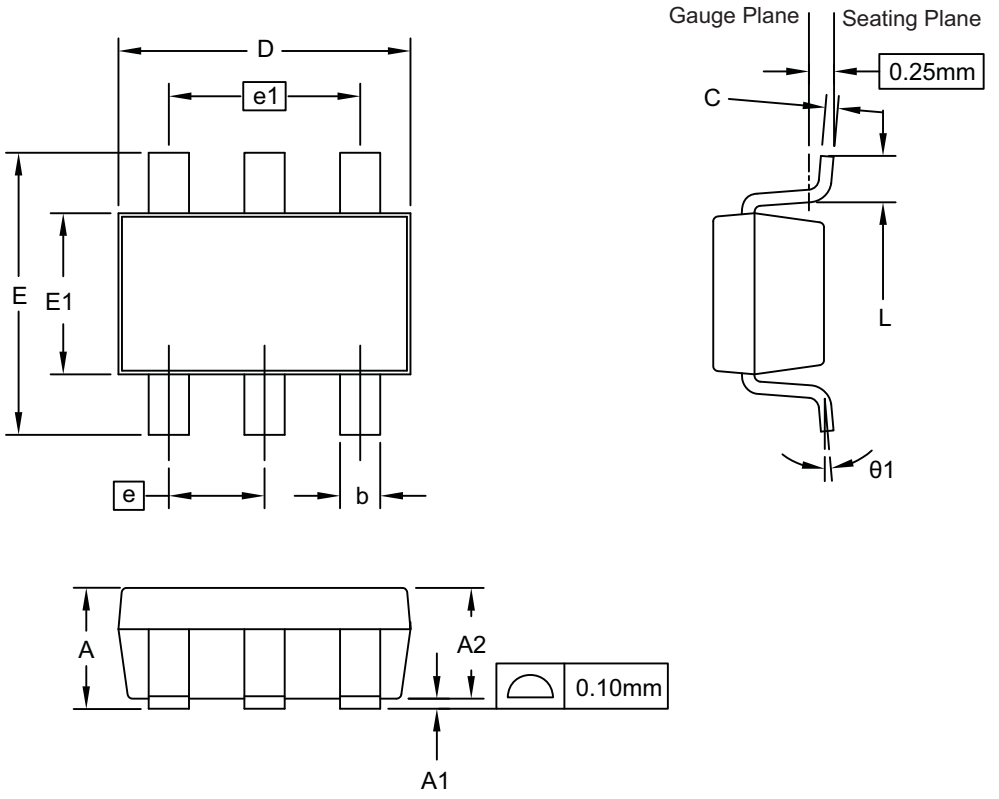
Minimize interconnecting line lengths by placing devices with the most interconnects as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground may cause ground bounce. The clamping performance of the TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage.

The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8300 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

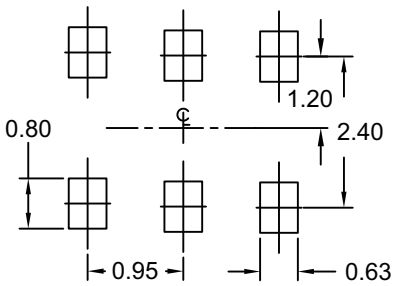
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio < 5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.

Package Dimensions, SOT23, 6L



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.90	—	1.25
A1	0.00	—	0.15
A2	0.70	1.10	1.20
b	0.30	0.40	0.50
C	0.08	0.13	0.20
D	2.70	2.90	3.10
E	2.50	2.80	3.10
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ	0°	—	8°

Dimensions in inches

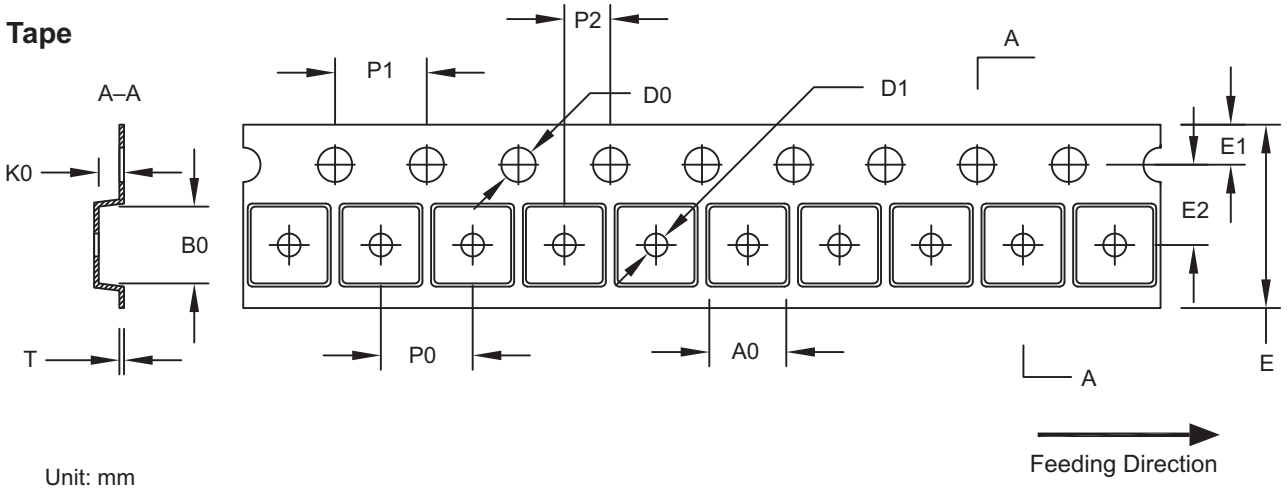
Symbols	Min.	Nom.	Max.
A	0.035	—	0.049
A1	0.000	—	0.006
A2	0.028	0.043	0.047
b	0.012	0.016	0.020
C	0.003	0.005	0.008
D	0.106	0.114	0.122
E	0.098	0.110	0.122
E1	0.059	0.063	0.067
e	0.037 BSC		
e1	0.075 BSC		
L	0.012	—	0.024
θ	0°	—	8°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils each.
2. Dimension “L” is measured in gauge plane.
3. Tolerance 0.100mm (4 mil) unless otherwise specified.
4. Followed from JEDEC MO-178C & MC-193C.
6. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOT23, 6L

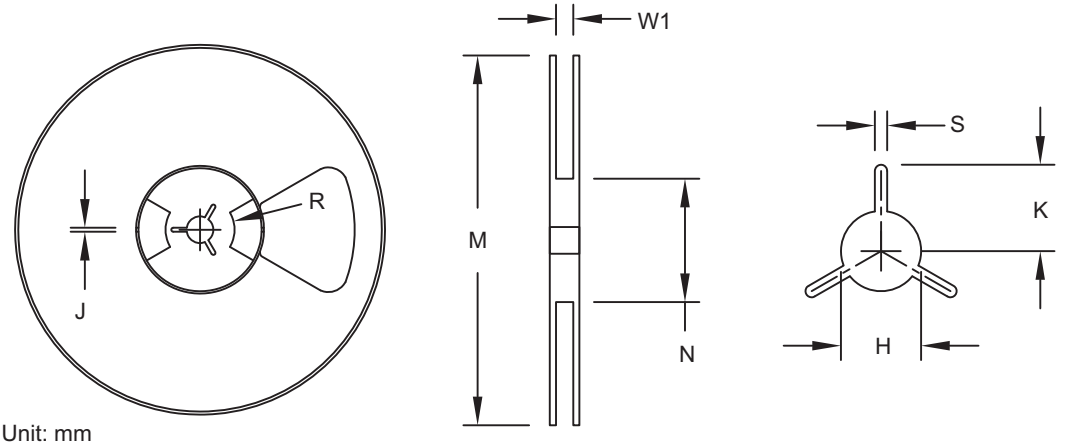
Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT-23	3.15 ±0.10	3.20 ±0.10	1.40 ±0.10	1.50 ±0.05	1.00 ±0.10/-0.0	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.23 ±0.03

Reel

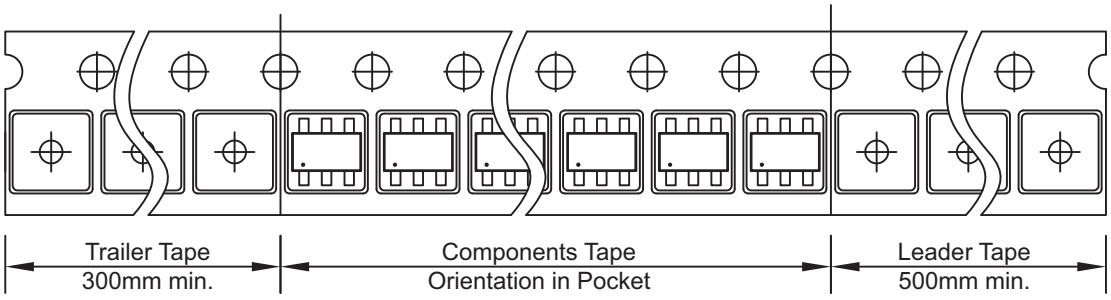


Unit: mm

Tape Size	Reel Size	M	N	W1	H	S	K	R	J
8 mm	ø177.80	ø177.80 MAX.	ø55.00 MIN.	8.40 +1.50/-0.00	ø13.00 +0.50 / -0.20	1.50 MIN.	10.10 MIN.	12.70	4.00 +0.10/-0.10

Leader/Trailer and Orientation

Unit Per Reel: 3000pcs



Part Marking

AOZ8300CI
(SOT-23)