MCR22-6, MCR22-8

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed and tested for repetitive peak operation required for CD ignition, fuel ignitors, flash circuits, motor controls and low−power switching applications.

Features

- 150 A for 2 μs Safe Area
- High dv/dt
- Very Low Forward “On” Voltage at High Current
- Low−Cost TO−226 (TO−92)
- Pb−Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (R_{GK} = IK, T_J = −40 to +110°C, Sine Wave, 50 to 60 Hz, R_{GK} = 1kΩ) MCR22−6 MCR22−8	V_{DRM}, V_{RRM}	 400 600	V
On−State Current RMS (180° Conduction Angles, T_C = 80°C)	$I_{T(RMS)}$	1.5	A
Peak Non−repetitive Surge Current, @T_A = 25°C, (1/2 Cycle, Sine Wave, 60 Hz)	I_{TSM}	15	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.9	A^2s
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T_A = 25°C)	P_{GM}	0.5	W
Forward Average Gate Power (t = 8.3 msec, T_A = 25°C)	$P_{G(AV)}$	0.1	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μs, T_A = 25°C)	I_{FGM}	0.2	A
Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μs, T_A = 25°C)	V_{RGM}	5.0	V
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	160	°C/W
Lead Solder Temperature (Lead Length ⩾ 1/16″ from case, 10 S Max)	T_L	+260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

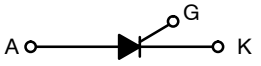
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

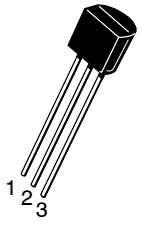
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

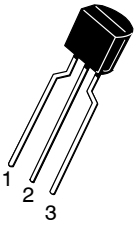
http://onsemi.com

SCRs
1.5 AMPERES RMS
400 thru 600 VOLTS





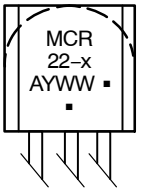
STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK

TO−92 (TO−226)
CASE 029
STYLE 10

MARKING DIAGRAMS



MCR22−x = Device Code
x = 6 or 8
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

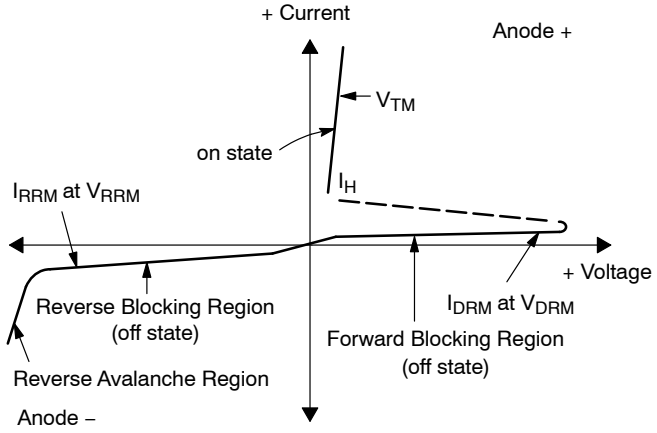
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}; R_{GK} = 1 kΩ)	T_C = 25°C T_C = 110°C	I_{DRM}, I_{RRM}	– –	– –	10 200	μA μA
ON CHARACTERISTICS						
Peak Forward On−State Voltage (Note 2) (I_{TM} = 1 A Peak)		V_{TM}	–	1.2	1.7	V
Gate Trigger Current (Continuous dc) (Note 3) (V_{AK} = 6 Vdc, R_L = 100 Ω)	T_C = 25°C T_C = −40°C	I_{GT}	– –	30 –	200 500	μA
Gate Trigger Voltage (Continuous dc) (Note 3) (V_{AK} = 7 Vdc, R_L = 100 Ω)	T_C = 25°C T_C = −40°C	V_{GT}	– –	– –	0.8 1.2	V
Gate Non−Trigger Voltage (V_{AK} = 12 Vdc, R_L = 100 Ω)	T_C = 110°C	V_{GD}	0.1	–	–	V
Holding Current (V_{AK} = 12 Vdc, R_{GK} = 1kΩ) Initiating Current = 20 mA	T_C = 25°C T_C = −40°C	I_H	– –	2.0 –	5.0 10	mA
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage (R_{GK} = 1kΩ) (T_C = 110°C)		dv/dt	–	25	–	V/μs

2. Pulse Width = 1.0 ms, Duty Cycle ≤ 1%.
3. R_{GK} Current not included in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



CURRENT DERATING

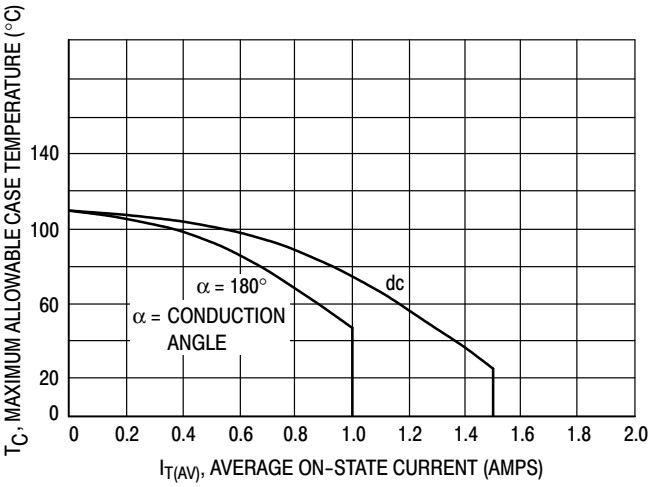


Figure 1. Maximum Case Temperature

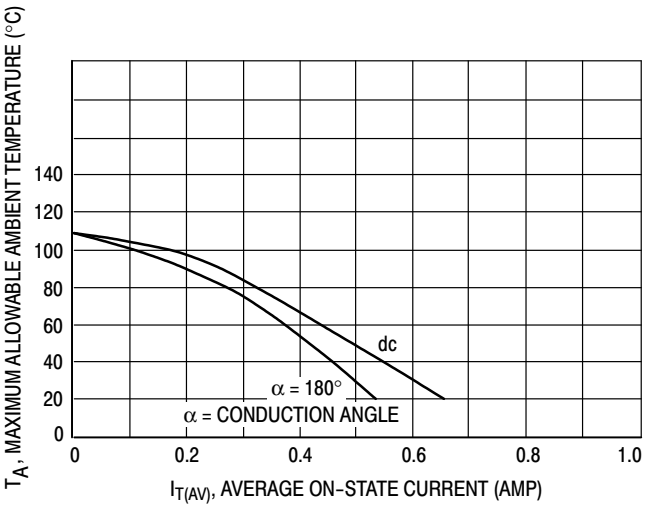


Figure 2. Maximum Ambient Temperature

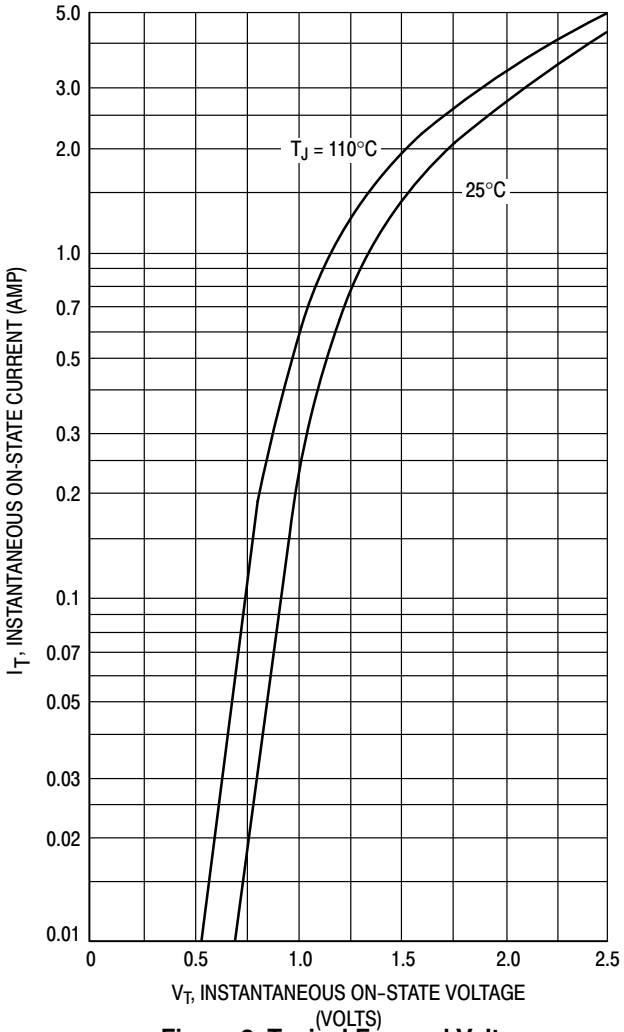


Figure 3. Typical Forward Voltage

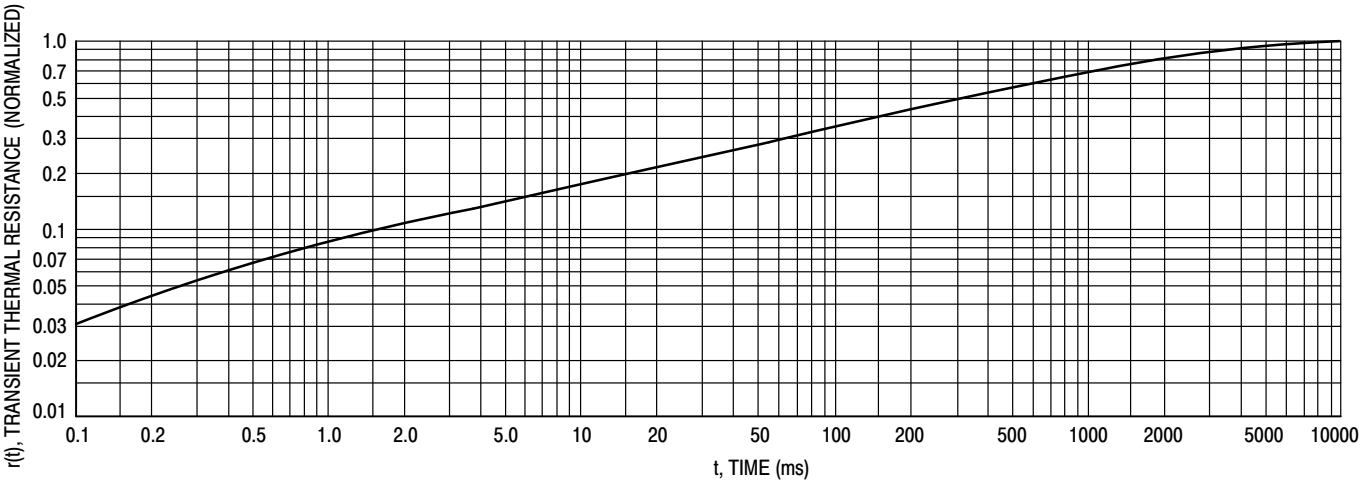


Figure 4. Thermal Response

TYPICAL CHARACTERISTICS

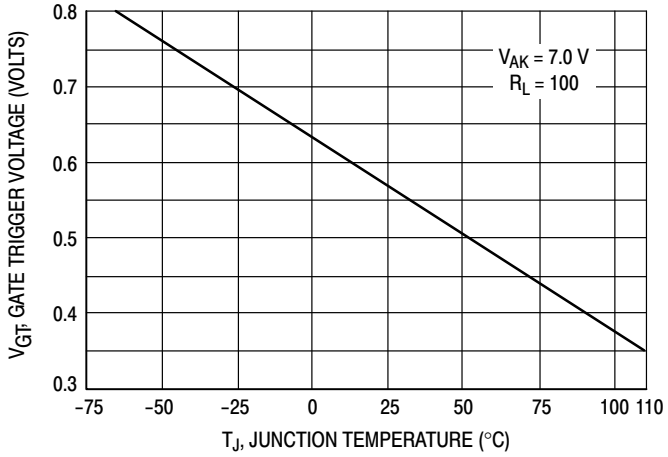


Figure 5. Typical Gate Trigger Voltage

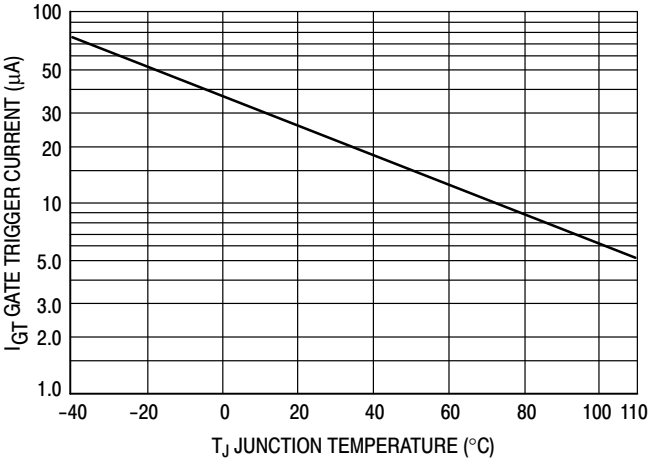


Figure 6. Typical Gate Trigger Current

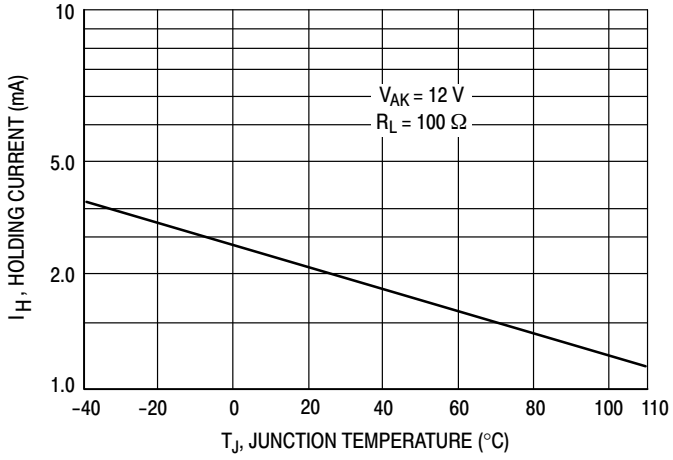


Figure 7. Typical Holding Current

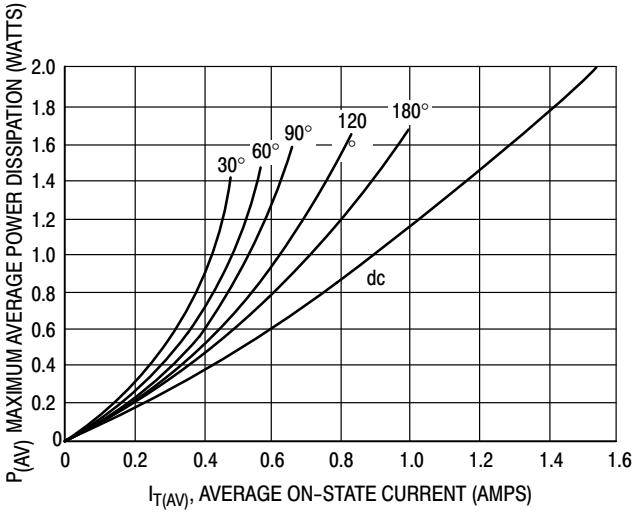


Figure 8. Power Dissipation

TO−92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

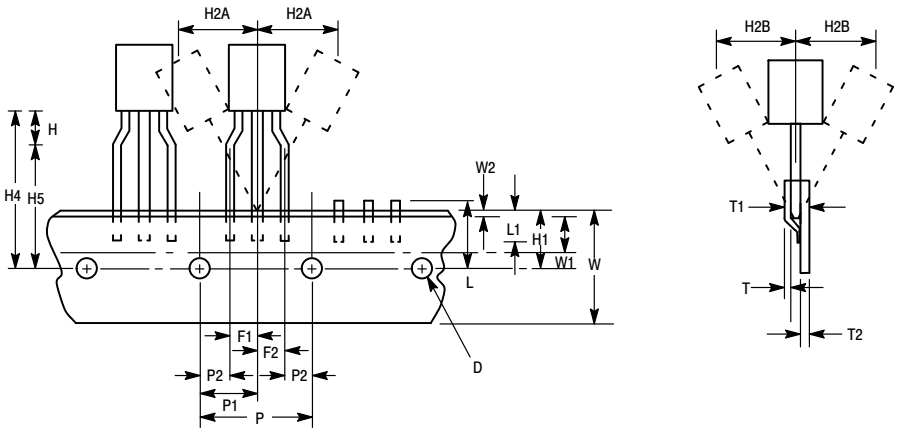


Figure 9. Device Positioning on Tape

Item	Symbol	Specification			
		Inches		Millimeter	
		Min	Max	Min	Max
Tape Feedhole Diameter	D	0.1496	0.1653	3.8	4.2
Component Lead Thickness Dimension	D2	0.015	0.020	0.38	0.51
Component Lead Pitch	F1, F2	0.0945	0.110	2.4	2.8
Bottom of Component to Seating Plane	H	.059	.156	1.5	4.0
Feedhole Location	H1	0.3346	0.3741	8.5	9.5
Deflection Left or Right	H2A	0	0.039	0	1.0
Deflection Front or Rear	H2B	0	0.051	0	1.0
Feedhole to Bottom of Component	H4	0.7086	0.768	18	19.5
Feedhole to Seating Plane	H5	0.610	0.649	15.5	16.5
Defective Unit Clipped Dimension	L	0.3346	0.433	8.5	11
Lead Wire Enclosure	L1	0.09842	–	2.5	–
Feedhole Pitch	P	0.4921	0.5079	12.5	12.9
Feedhole Center to Center Lead	P1	0.2342	0.2658	5.95	6.75
First Lead Spacing Dimension	P2	0.1397	0.1556	3.55	3.95
Adhesive Tape Thickness	T	0.06	0.08	0.15	0.20
Overall Taped Package Thickness	T1	–	0.0567	–	1.44
Carrier Strip Thickness	T2	0.014	0.027	0.35	0.65
Carrier Strip Width	W	0.6889	0.7481	17.5	19
Adhesive Tape Width	W1	0.2165	0.2841	5.5	6.3
Adhesive Tape Position	W2	.0059	0.01968	.15	0.5

NOTES:

1. Maximum alignment deviation between leads not to be greater than 0.2 mm.
2. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
3. Component lead to tape adhesion must meet the pull test requirements.
4. Maximum non−cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
5. Holddown tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
6. No more than 1 consecutive missing component is permitted.
7. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
8. Splices will not interfere with the sprocket feed holes.

ORDERING & SHIPPING INFORMATION: MCR22 Series Packaging Options, Device Suffix

U.S.	Europe Equivalent	Shipping†	Description of TO−92 Tape Orientation
	MCR22−8RL1	2000 / Tape & Reel	Flat side of TO−92 and adhesive tape visible
	MCR22−8RL1G		
MCR22−6		5000 Units / Box	N/A, Bulk
MCR22−6G			
MCR22−8			
MCR22−8G			
MCR22−6RLRA		2000 / Tape & Reel	Round side of TO−92 and adhesive tape visible
MCR22−6RLRAG			
MCR22−6RLRP		2000 / Tape & Ammo Pack	Flat side of TO−92 and adhesive tape visible
MCR22−6RLRPG			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

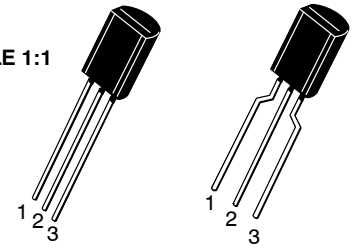
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

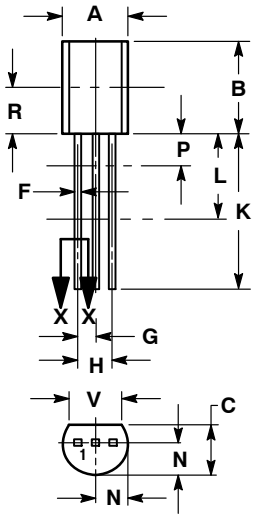
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

SCALE 1:1



STRAIGHT LEAD BENT LEAD



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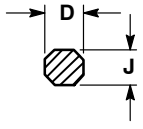
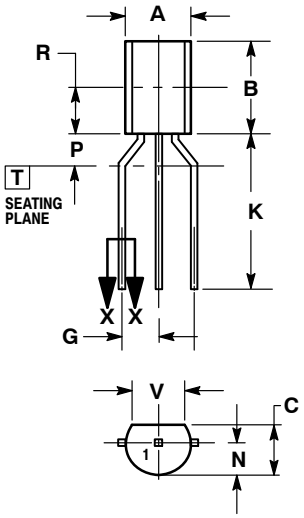


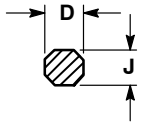
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
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B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 2**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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