STD80N4F6, STU80N4F6

N-channel 40 V, 5.5 mΩ typ., 80 A STripFET™ VI DeepGATE™ Power MOSFET in DPAK and IPAK packages

Datasheet – production data

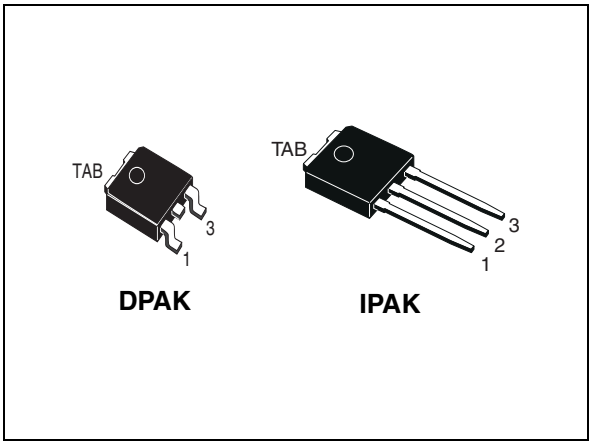
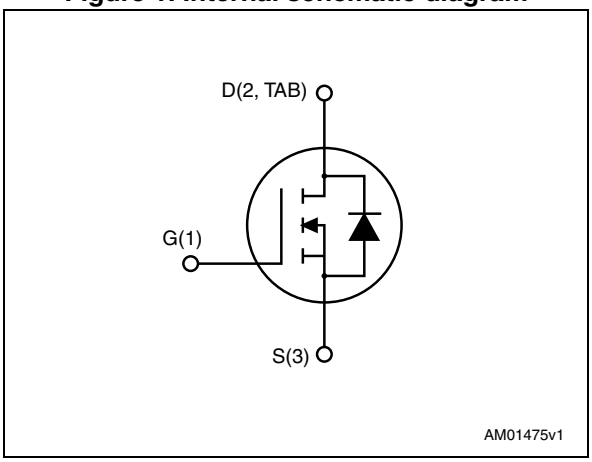


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STD80N4F6	40 V	6.0 mΩ	80 A
STU80N4F6		6.3 mΩ	

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFETs exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD80N4F6	80N4F6	DPAK	Tape and reel
STU80N4F6		IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80 (1)	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	56 (1)	A
I_{DM} (2)	Drain current (pulsed)	320 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
I_{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{Jmax})	40	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	149	mJ
	Derating factor	0.47	W/°C
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		°C

1. Current limited by package.
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.14		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		100	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient max	50		°C/W

1. When mounted on FR-4 board of inch^2, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 40 V V_{DS} = 40 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A for DPAK for IPAK		5.5 5.8	6 6.3	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2150	-	pF
C_{oss}	Output capacitance		-	335	-	pF
C_{rss}	Reverse transfer capacitance		-	160	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 80 A, V_{GS} = 10 V (see *Figure 14*)	-	36	-	nC
Q_{gs}	Gate-source charge		-	11	-	nC
Q_{gd}	Gate-drain charge		-	9	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	10.5	-	ns
t_r	Rise time		-	7.6	-	ns
t_d(off)	Turn-off delay time		-	46.1	-	ns
t_f	Fall time		-	11.9	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM} (1)	Source-drain current (pulsed)		-		320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, di/dt = 100 A/µs V_{DD} = 32 V (see *Figure 17*)	-	41.1		ns
Q_{rr}	Reverse recovery charge		-	43.6		nC
I_{RRM}	Reverse recovery current		-	2.1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

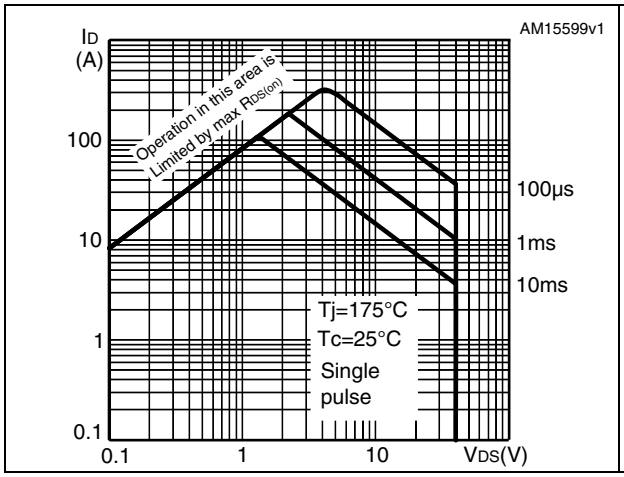


Figure 3. Thermal impedance

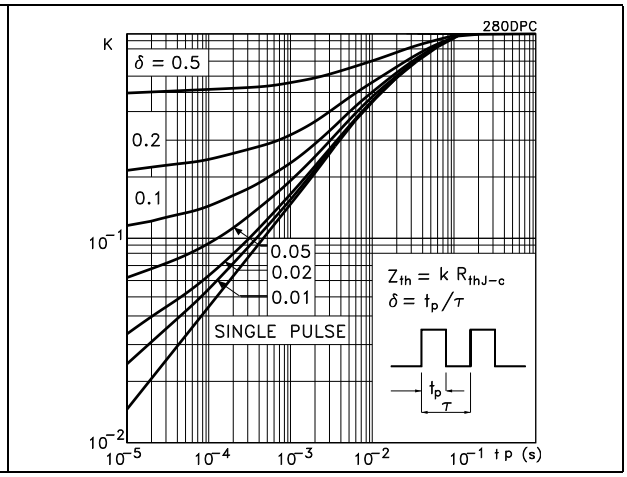


Figure 4. Output characteristics

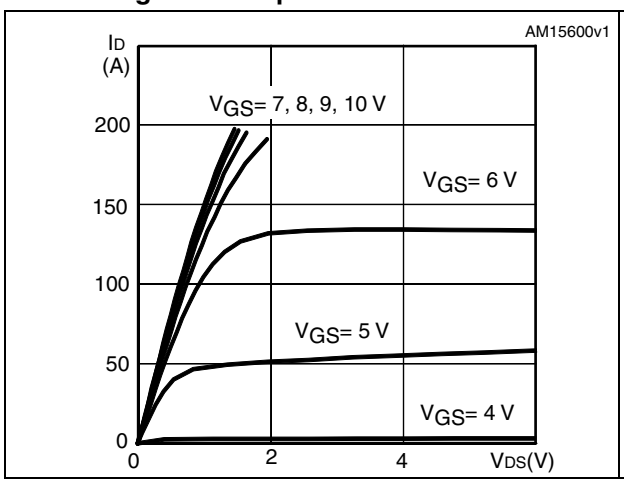


Figure 5. Transfer characteristics

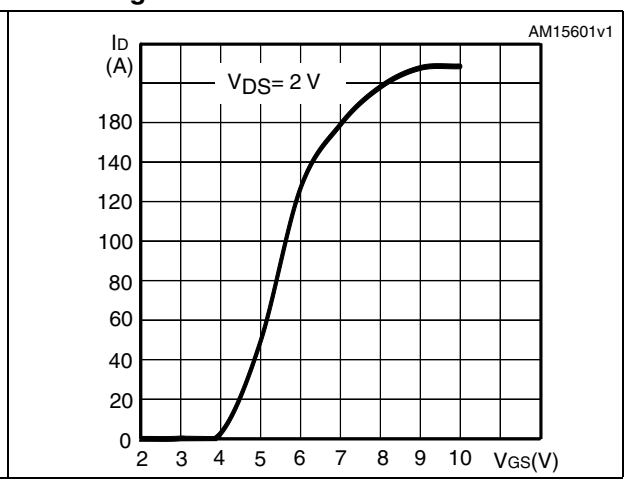


Figure 6. Gate charge vs gate-source voltage

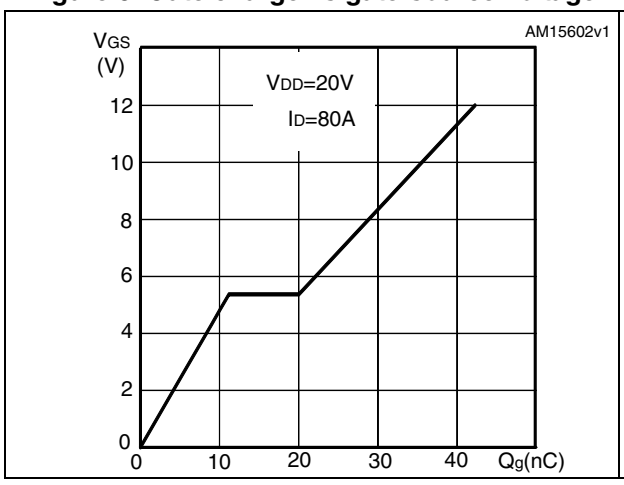


Figure 7. Static drain-source on-resistance

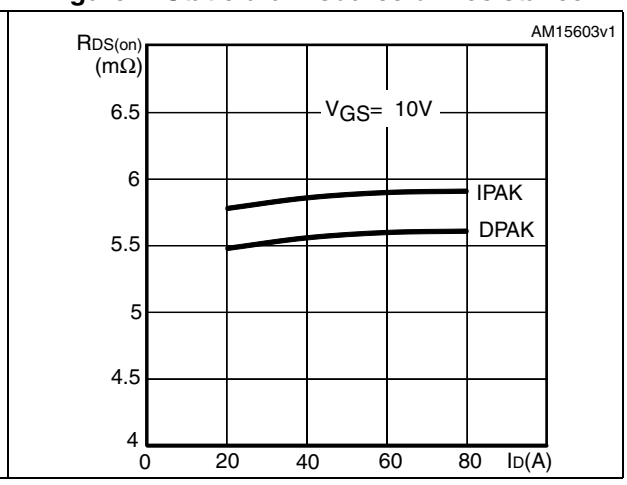


Figure 8. Capacitance variations

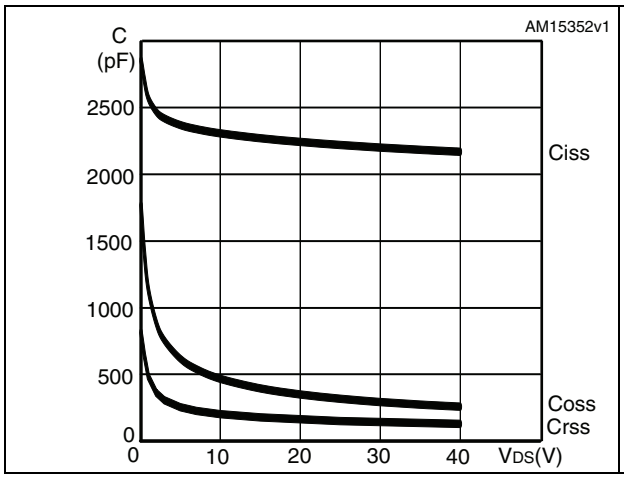


Figure 9. Drain-source diode forward characteristics

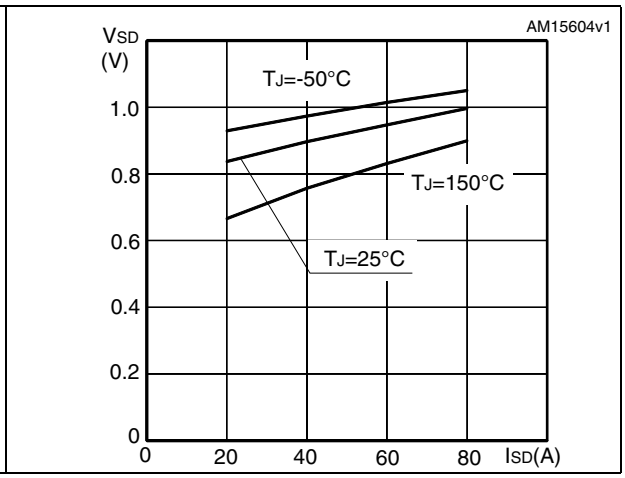


Figure 10. Normalized gate threshold voltage vs temperature

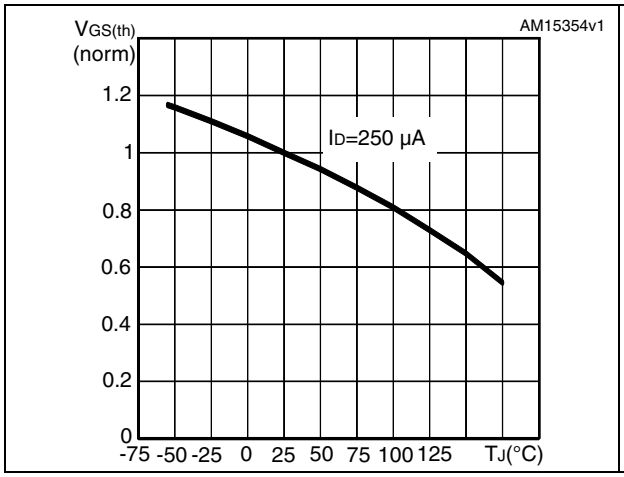


Figure 11. Normalized on-resistance vs temperature

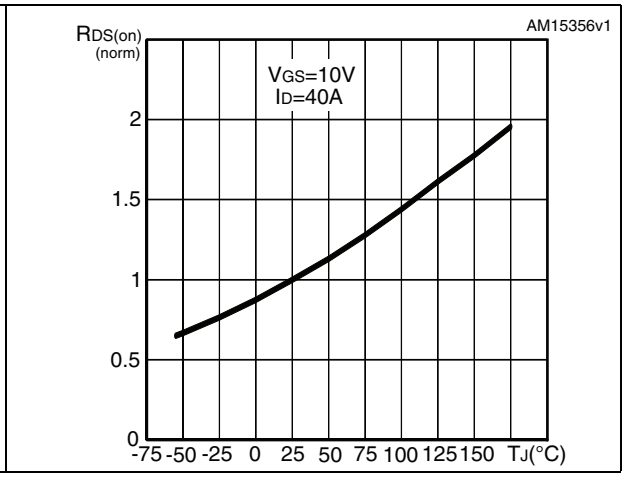
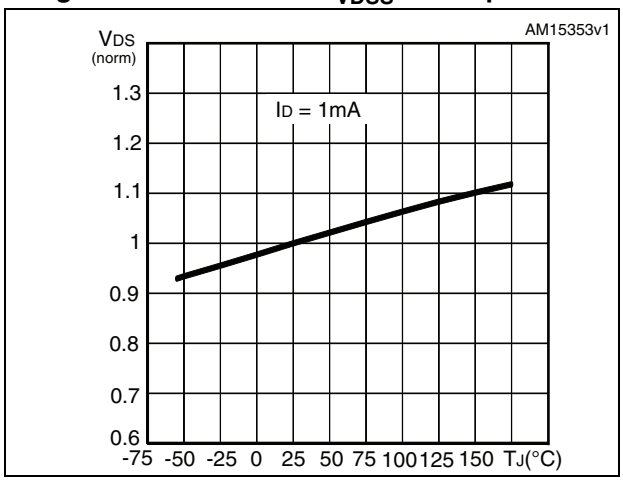


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

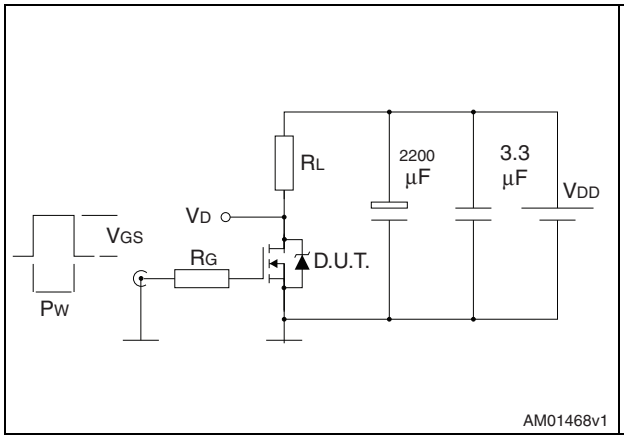


Figure 14. Gate charge test circuit

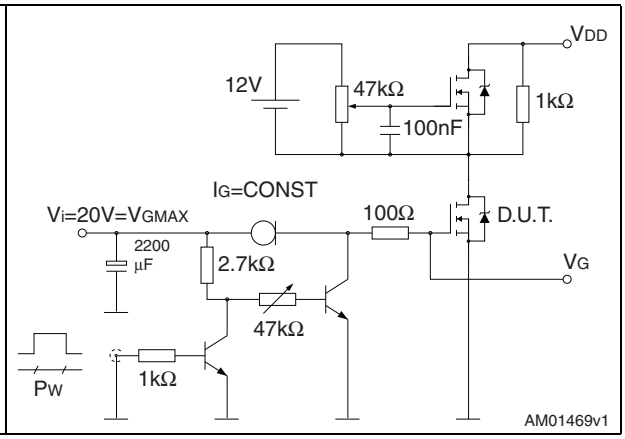


Figure 15. Test circuit for inductive load switching and diode recovery times

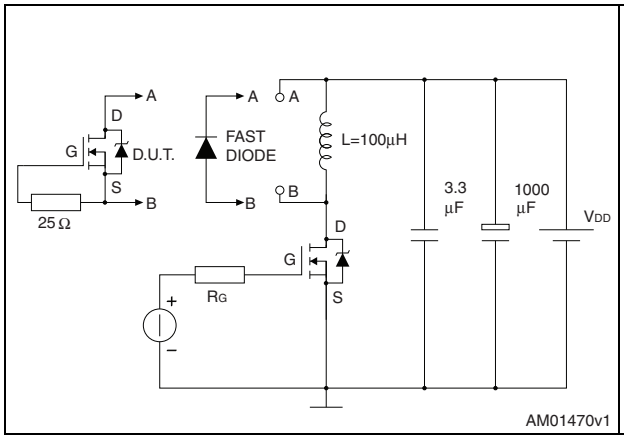


Figure 16. Unclamped inductive load test circuit

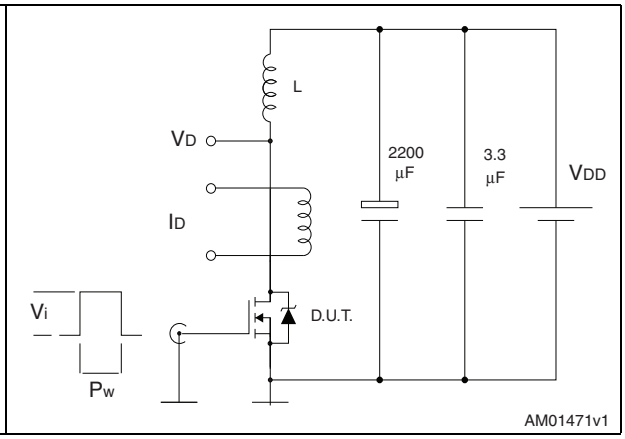


Figure 17. Unclamped inductive waveform

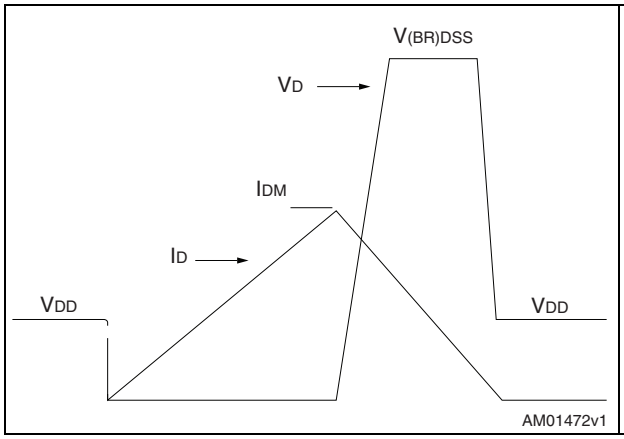
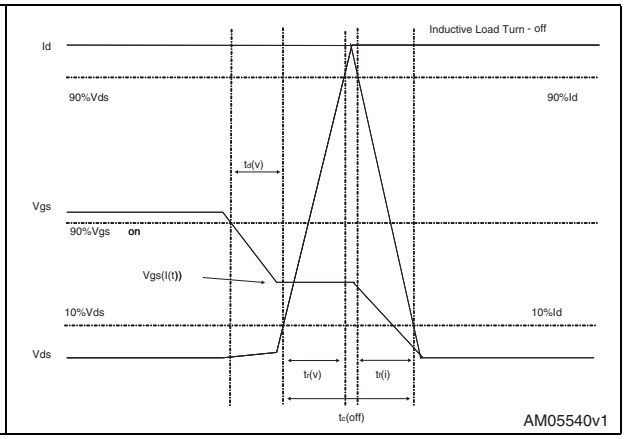


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19. DPAK (TO-252) drawing

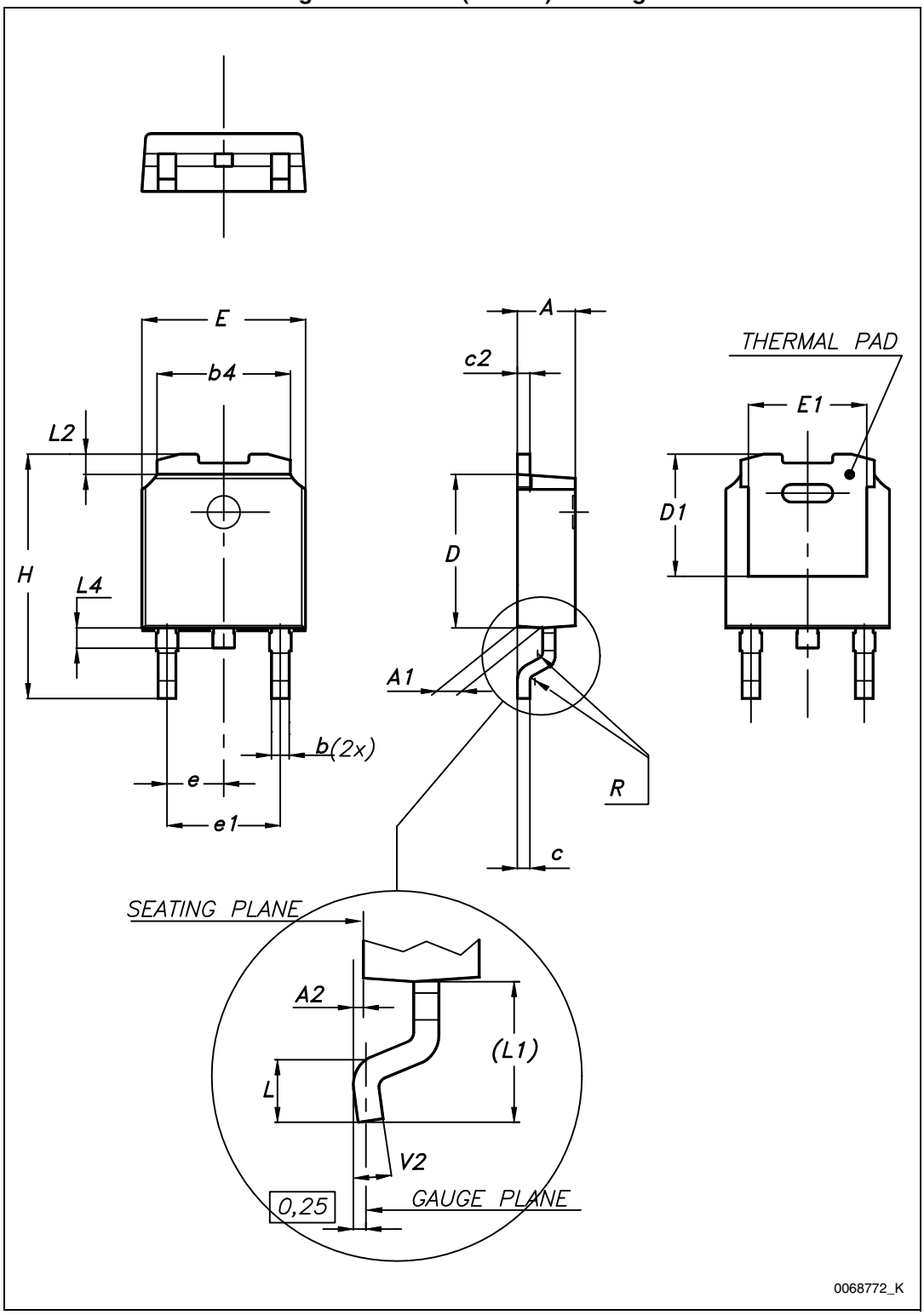
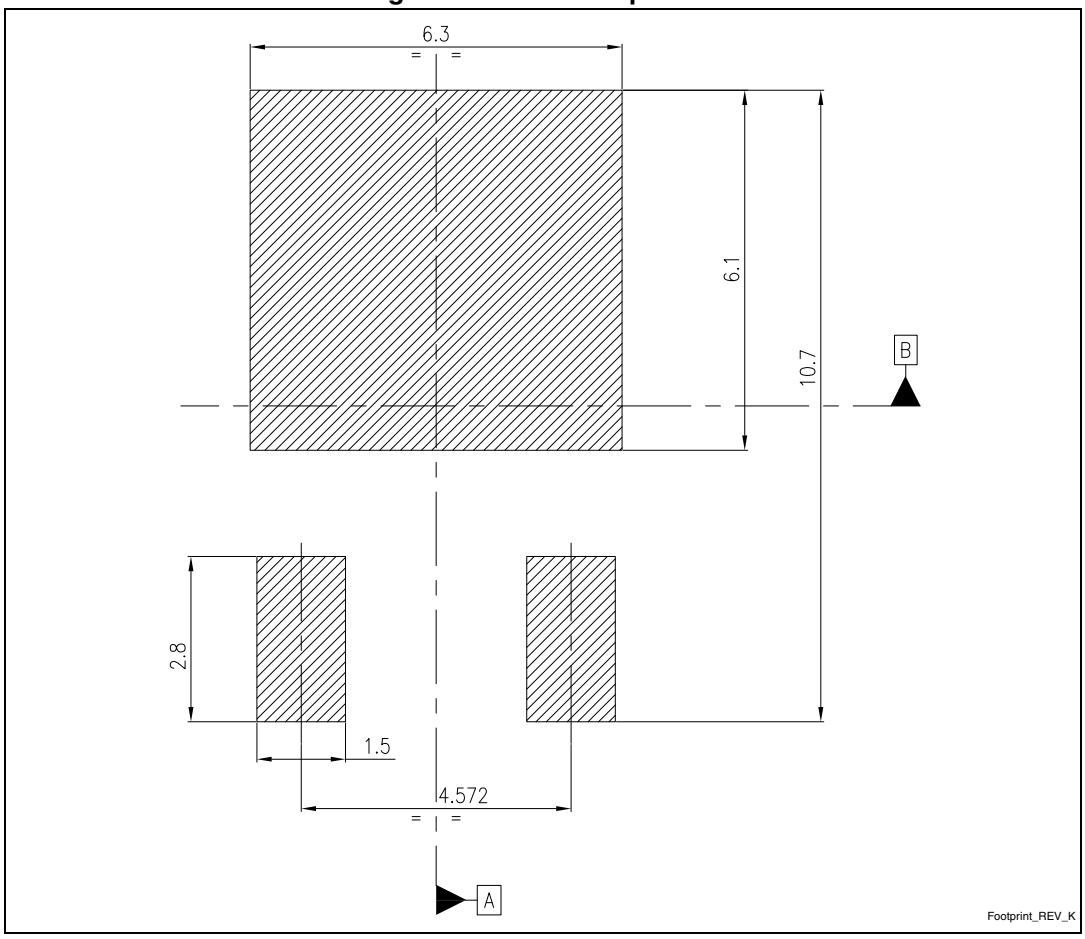


Figure 20. DPAK footprint [(a)]

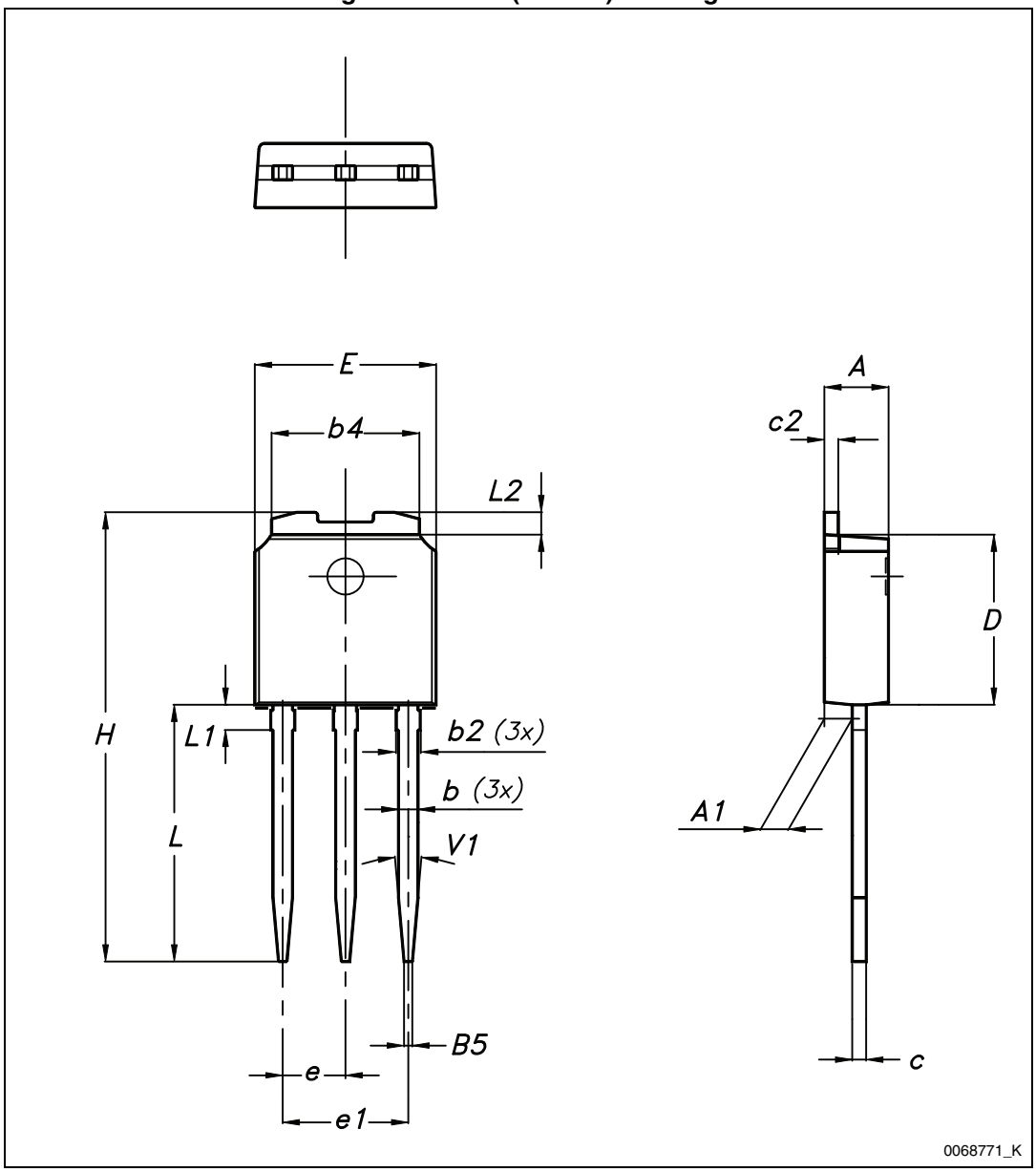


a. All dimensions are in millimeters

Table 9. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 21. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

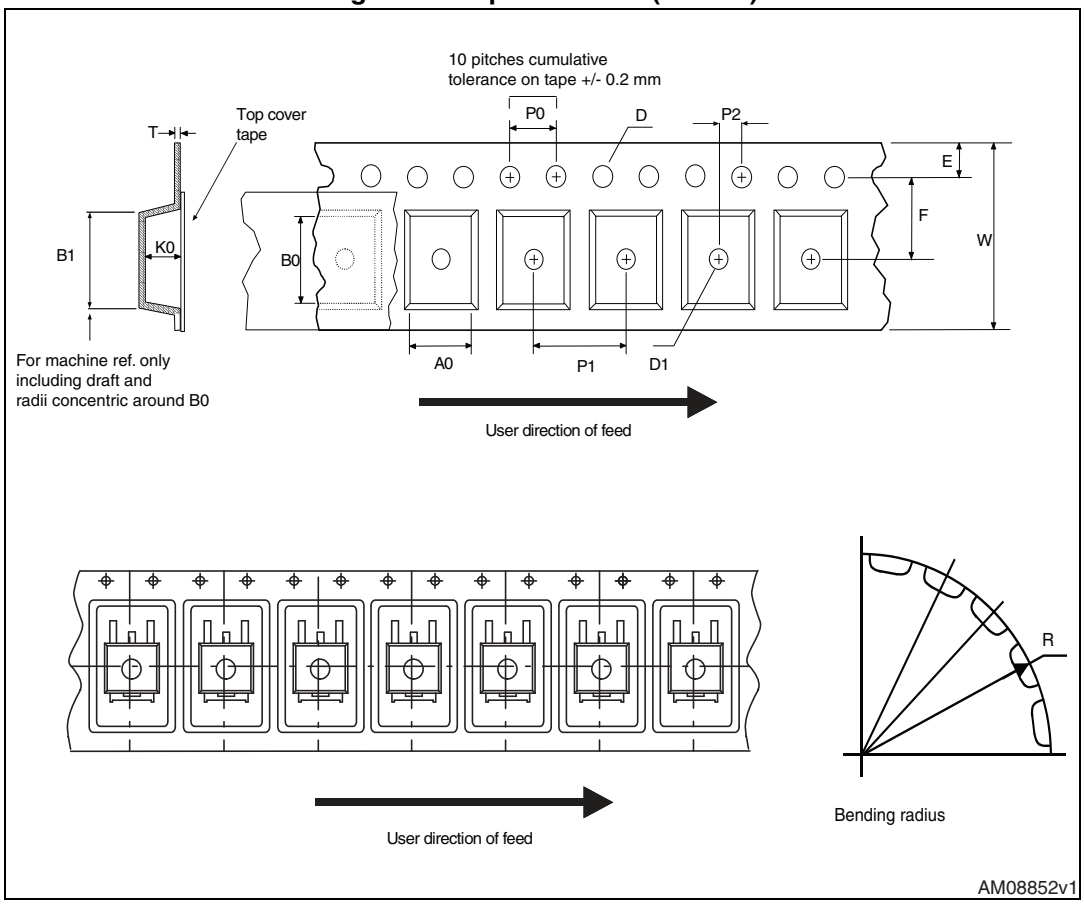
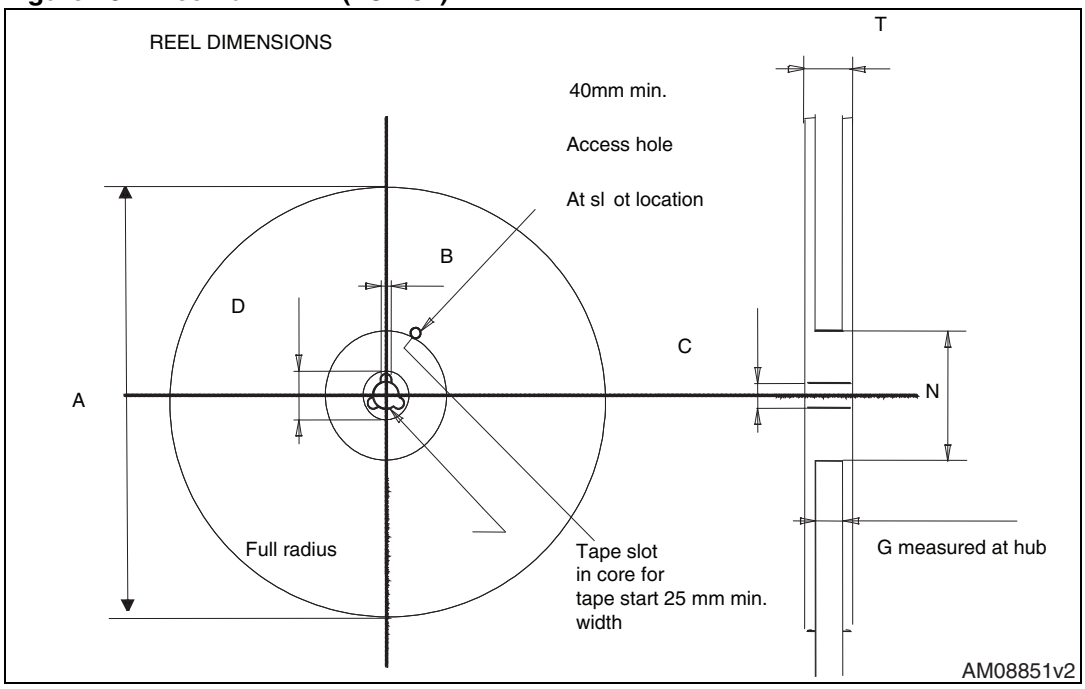


Figure 23. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
26-Oct-2012	1	Initial release.
01-Mar-2013	2	– Added: IPAK package – The part number STI80N4F6 has been moved to a separate datasheet – Added: *Figure 2*, *3*, *4*, *5*, *6*, *7* and *9*
05-Mar-2013	3	– Minor text changes – Modified: *Table 3*